

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application.

LISTING OF CLAIMS:

What is claimed is:

1 1. (Currently Amended) A method for providing an area
2 optimized binary orthogonality checker for a scalable
3 selector system for controlling data transfers and routing
4 in a data processing system comprising the steps of:
5 determining ~~the~~ gate count for an implementation of an
6 optomized orthogonality checker, ~~17~~ and minimizing the logical
7 gate count for an implementation of ~~an~~ said orthogonality
8 checker given a library of logical gates to implement a
9 minimized ~~the~~ circuit and the area for each logical gate in
10 the library.

1 2. (Currently Amended) The method according to claim 1
2 including the steps of:
3
4 ~~determining the~~ establishing an optimal mix of hierarchical
5 level ~~17~~ and
6
7 determining the inputs to implement said a-given
8 orhogonality checker ~~to achieve the~~ for said minimized
circuit.

1 3. (Currently Amended) The method according to claim 1,
2 where the area of ~~a binary~~ said orthogonality checker is
3 implemented in a static CMOS circuits by minimizing the
4 logical gate count and area needed for checker
5



6 implementation given a library of logical gates to implement
7 the circuit and the area for each gate in the library.

1 4. (Currently Amended) The method according to claim 3,
2 including a step of determining establishing an optimal mix
3 of hierarchical levels and inputs to implement ~~a given said~~
4 orthogonality checker to achieve ~~the~~ said minimized circuit.

1 5. (Currently Amended) The method according to claim 4
2 wherein said orthogonality checker is employed in a scalable
3 selector system for controlling data transfers and routing
4 in a data processing system, comprising a plurality of input
5 data buses coupled to a multiple-bit, multiple bus selector
6 having data, data valid, and outputs of an orthogonality
7 checker ~~outputs~~ and having multiple data input bus ports
8 coupled for receipt of signal from said plurality of input
9 data buses.

1 6. (Currently Amended) ~~The A~~ method employed in a data
2 processing system having a plurality of input data buses
3 coupled to a multiple-bit, multiple bus selector having
4 data, data valid, and outputs of an orthogonality checker
5 and having multiple data input bus ports coupled for receipt
6 of signal from said plurality of input data buses according
7 to claim 5 wherein after comprising the steps of:
8 determining establishing an expected number for ~~the a~~
9 logical gate count for an implementation of an orthogonality
10 checker, and providing the binary orthogonality checking ~~is~~
11 provided by hierarchically combining the checks outputs of
said orthogonality checker with smaller numbers of inputs



12 and performing the total check of a large number of inputs
13 with less gates and in a smaller area.

1 7. (Currently Amended) The method according to claim 6
2 wherein after determining an expected number for the logical
3 gate count, then providing multiple checks with reduced
4 input sets are combined into one larger check and the
5 orthogonality checking is performed, with a check on each
6 input set, as well as with combining an OR of all the inputs
7 for providing resulting OR values to the one larger check.

1 8. (Original) The method according to claim 7 wherein the
2 resulting OR values are then checked for orthogonality, and
3 the results of all the checks are ORed together.

1 9. (Currently Amended) The method according to claim 8
2 wherein ~~the structure for~~ orthogonality checker is extended
3 to multiple hierarchical levels and works with orthogonality
4 checks for an ~~said~~ extended size of implementation.

1 10. (Currently Amended) The method according to claim 9
2 wherein the orthogonality checker ~~structure determined is~~
3 has an optimal hierarchical structure for a given
4 technology library and a given number of inputs to check.